# IBM PowerPC 970 Overview

## Session 502

# IBM PowerPC 970 Overview

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# What You'll Learn

- Principle features of the PowerPC 970 processor
- Block diagram level description
- Instruction processing
- Address translation
- Data processing
- Computation
- L2 and bus interface

# PowerPC 970 Features

- Based on the award-winning POWER4 design
- High-performance microprocessor
  - 2 GHz, superscalar
  - Out-of-order execution
- 64-bit implementation
  - 32-bit compatible
- SIMD enhanced
  - Velocity Engine, data prefetch
- High Memory and I/O bandwidth
  - 1 GHz bus, 8 GBps peak bandwidth

# PowerPC 970 Block Diagram

BIU – Bus interface unit

L2 – Second level cache

L1 – First level instruction or data cache

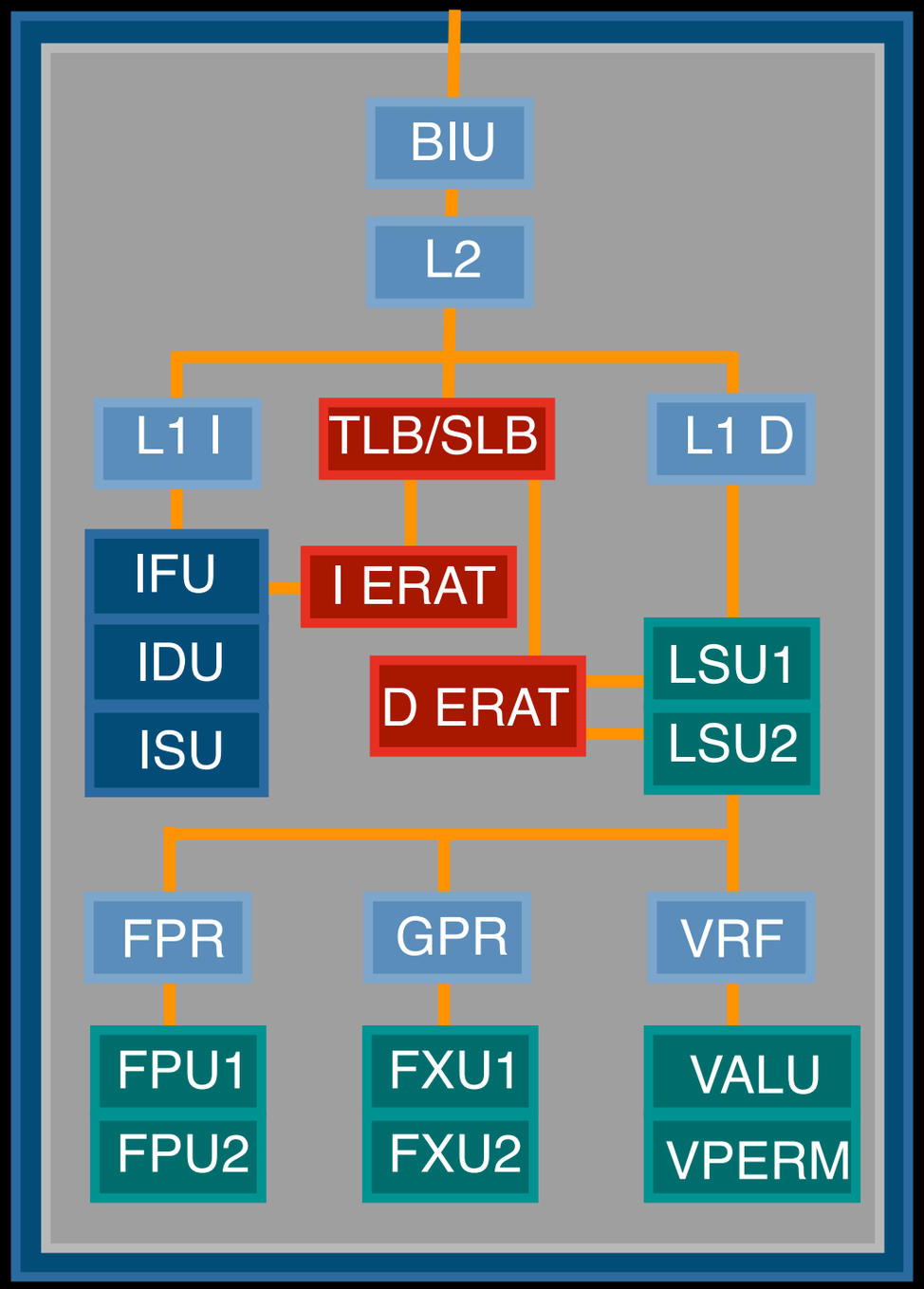
IFU – Instruction fetch unit

IDU – Instruction decode unit

ISU – Instruction sequencer unit

TLB – Table lookaside buffer

SLB – Segment lookaside buffer




ERAT – Instruction or data effective to real address translation table

LSU – Load-store unit

FPR – Floating point registers

GPR – General purpose registers

VRF – Vector register file

FPU – Floating point unit

FXU – Fixed point unit

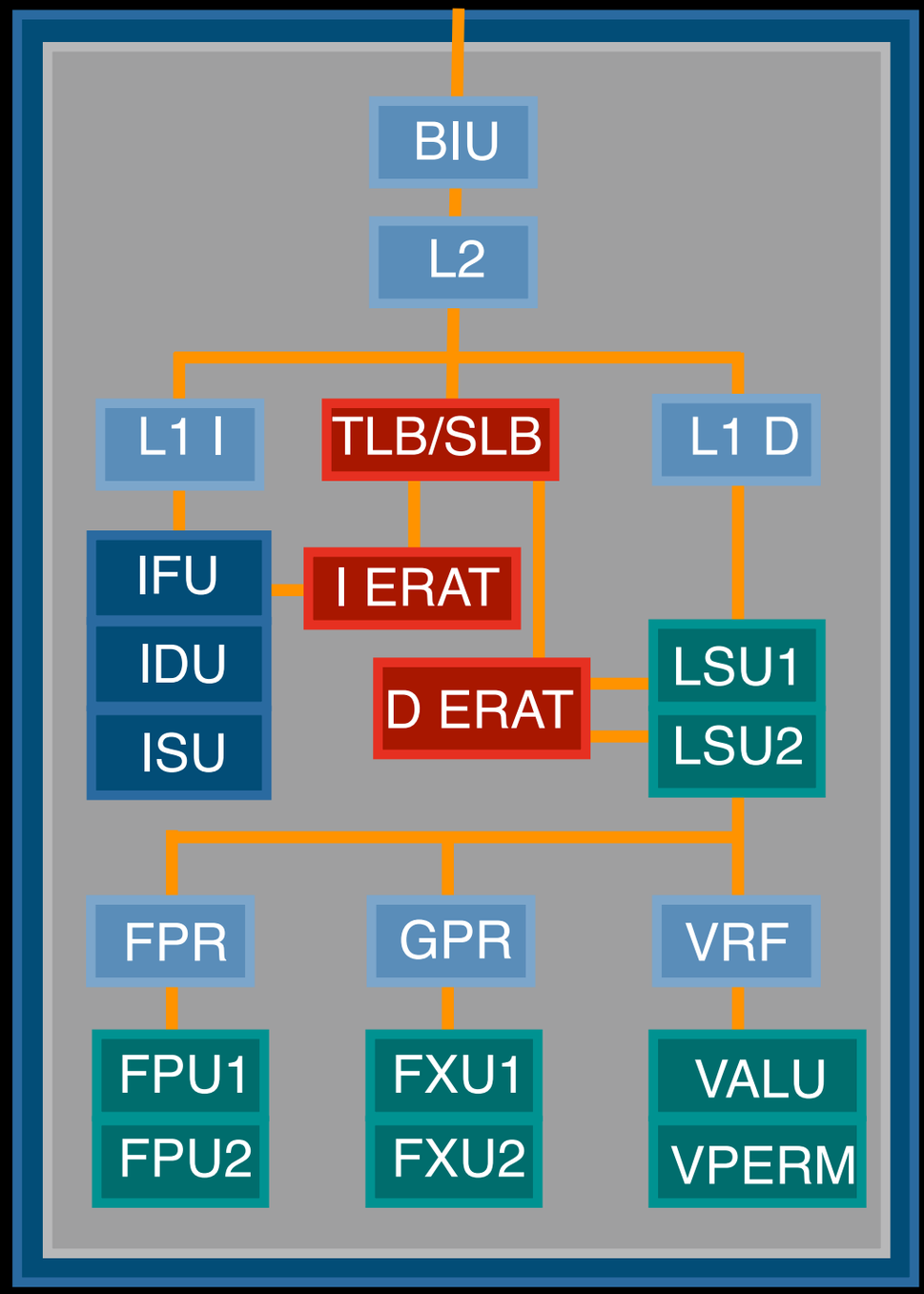
VALU – Vector arithmetic logic unit

VPERM – Vector permute unit

# PowerPC 970 Features

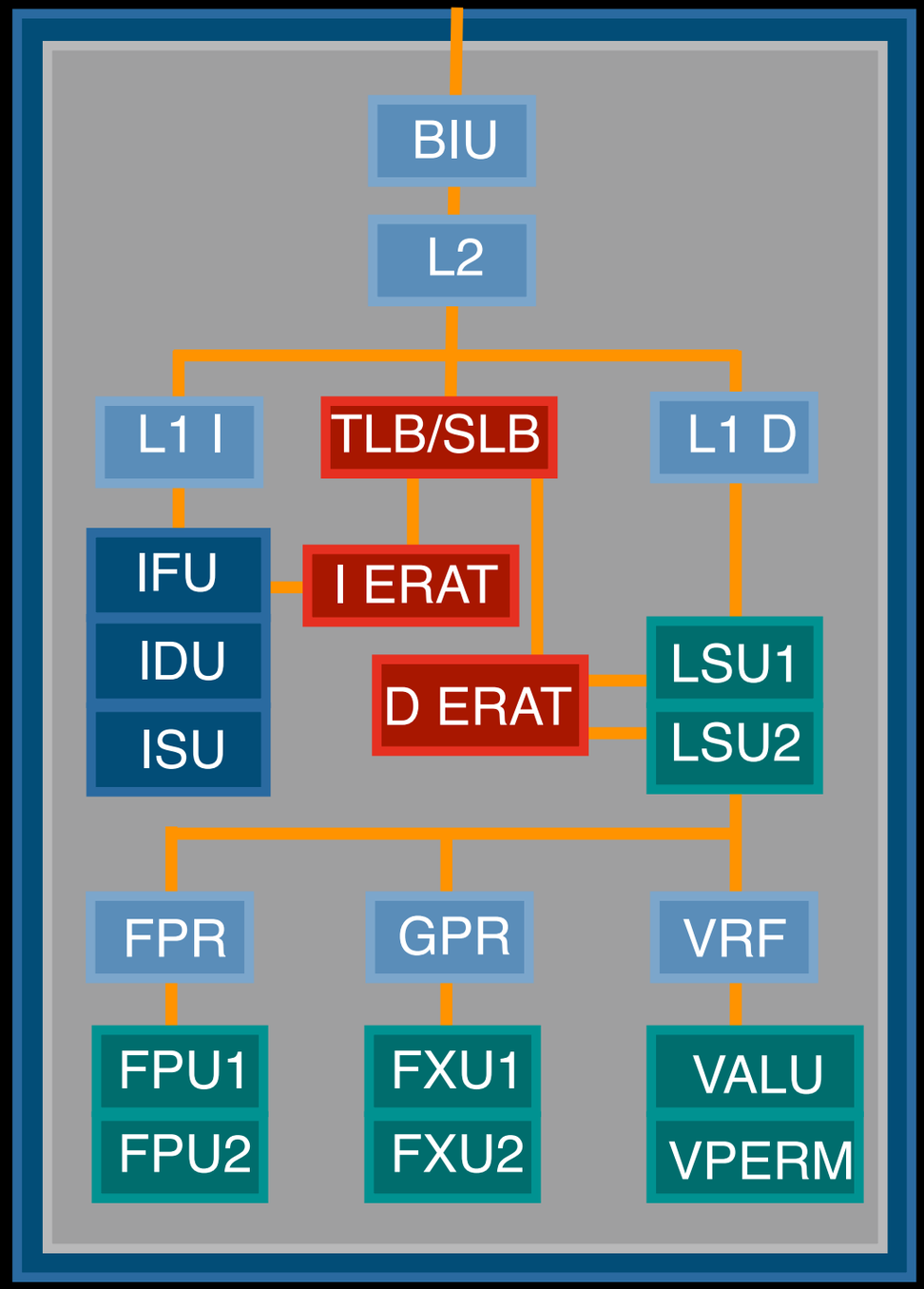
- Instruction pipe
  - 64KB L1 Inst cache, direct□mapped
  - 32 entry I buffer
  - 8 instructions fetch / cycle
  - Up to 5 dispatch / cycleUp to 10□ssue / cycle
  - Over 200 instructions in-flight

- Data pipe
  - 32 KB L1 Data cache, 2-way sa
  - 512KB L2 cache, 8-way sa
  - 8 data prefetch streams

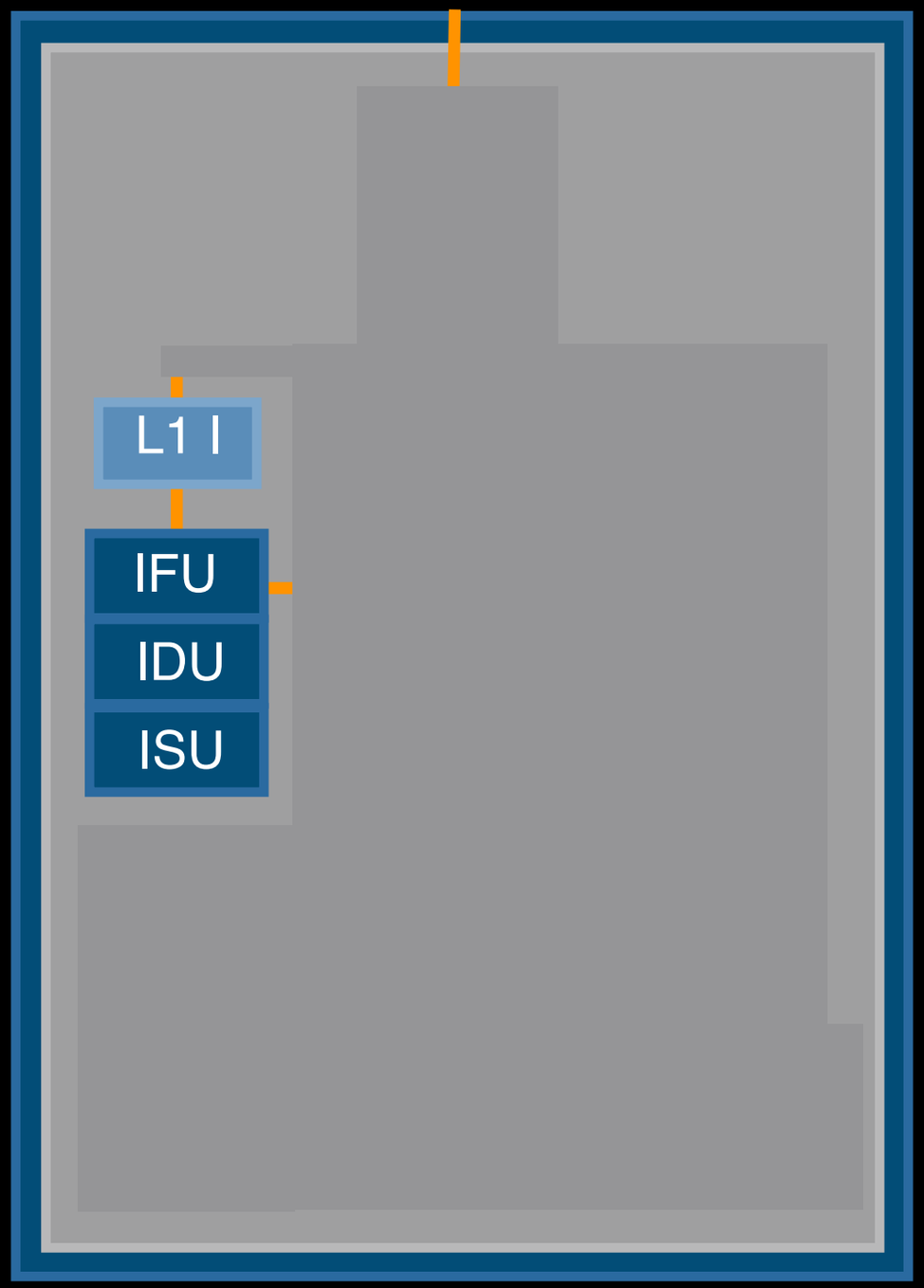


# PowerPC 970 Features

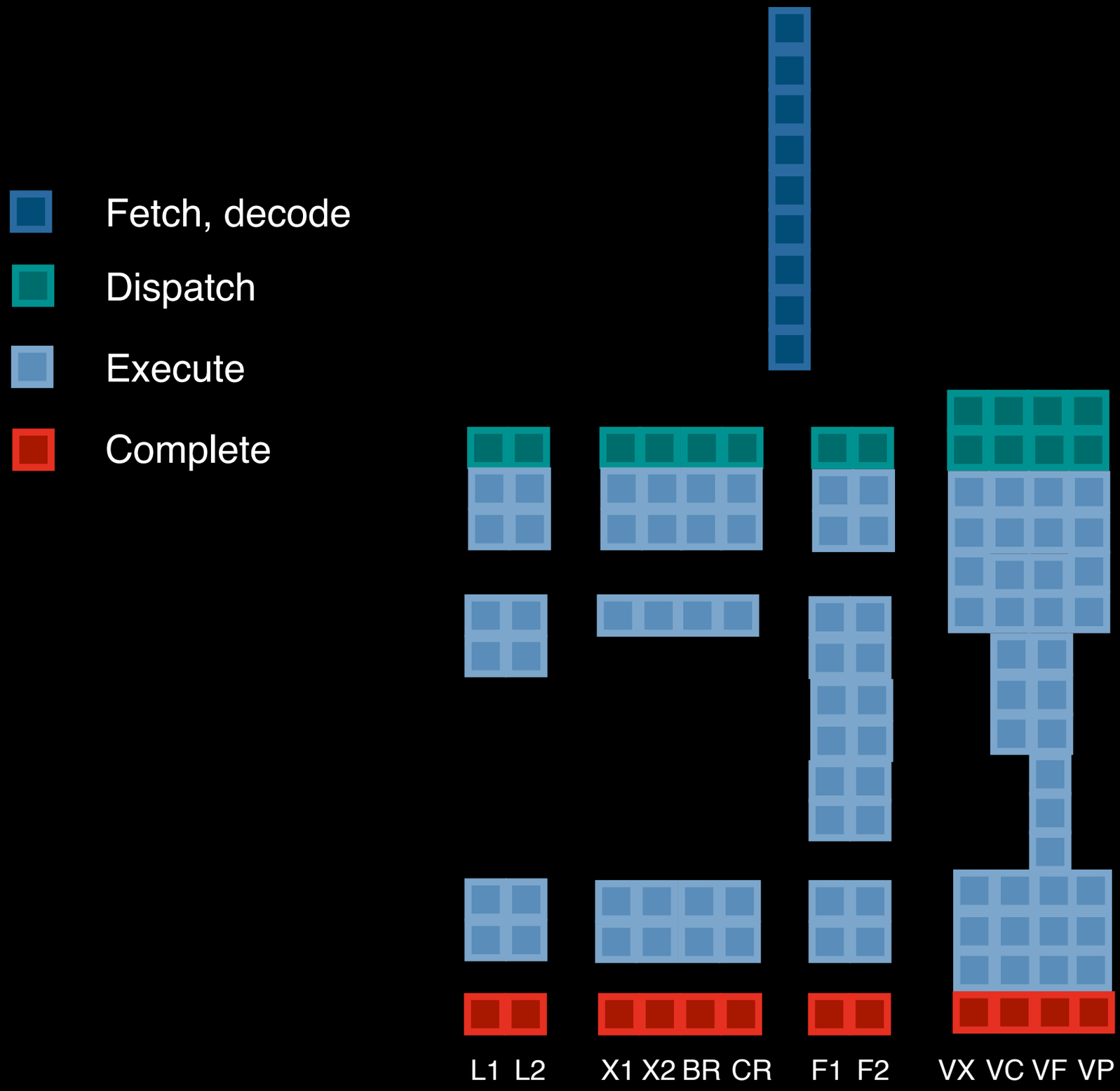
- Memory management
  - 64 entry SLB, fully associative
  - 256 x 4-way TLB
  - 64 x 2-way Inst and Data ERATs
  - Supports 42-bit real addresses
  -
- Execution
  - 2 Load/store units
  - 2 Fixed point units
  - 2 IEEE floating point units
  - 2 SIMD units—VALU, VPERM
  - Branch unit
  - Condition register unit



# Instruction Processing



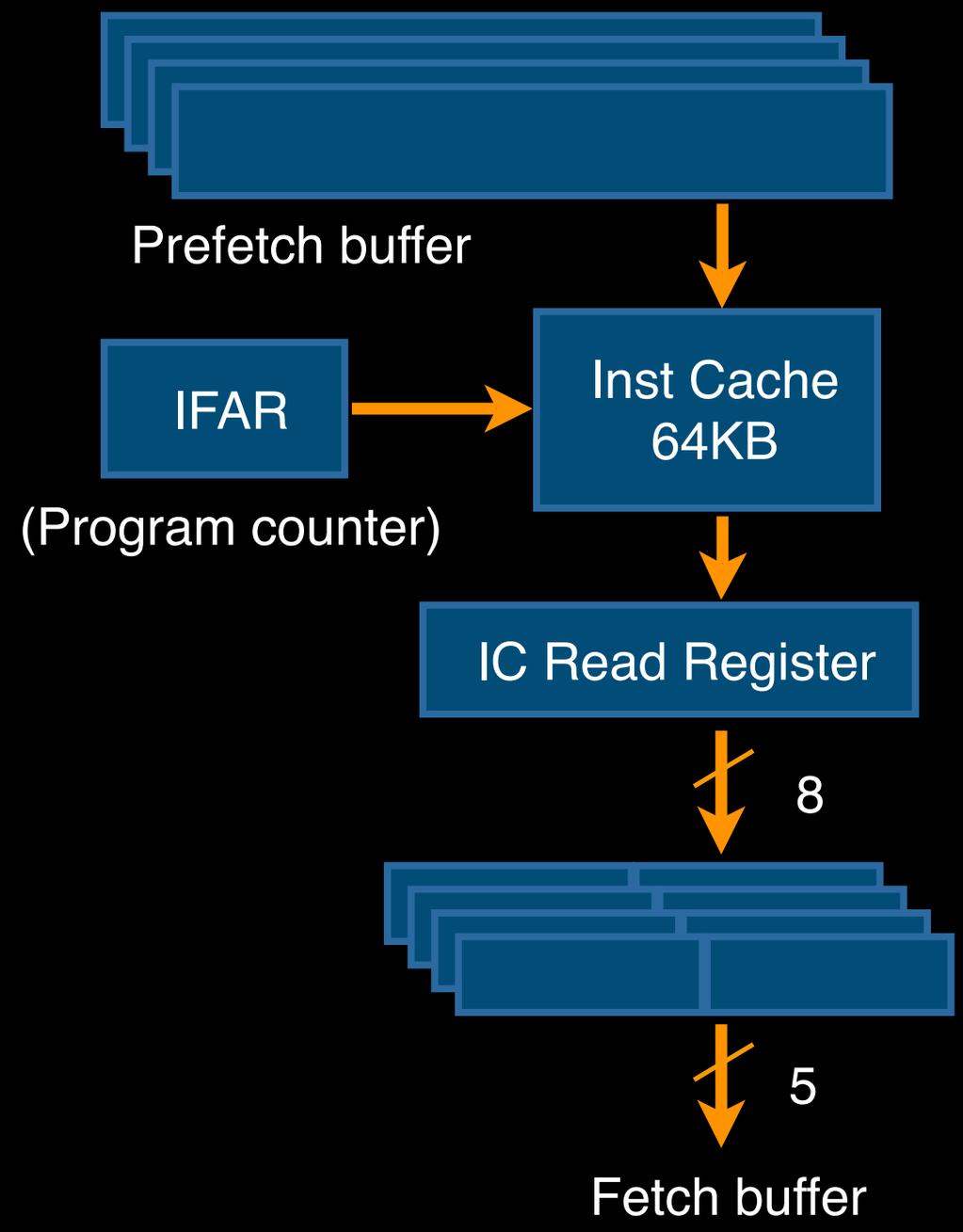
# PowerPC 970 Pipeline



# Instruction Fetch

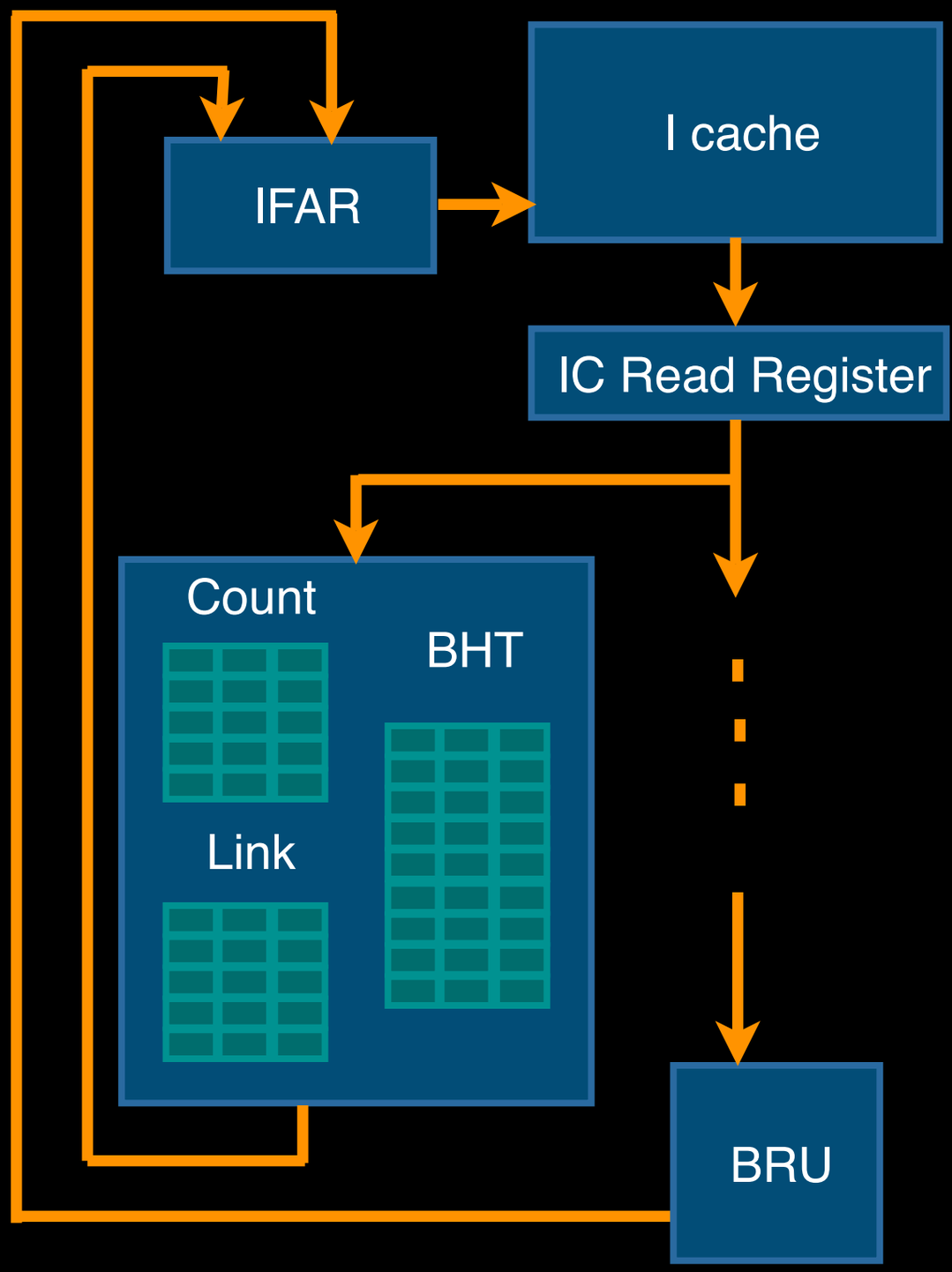
- 64KB L1 I cache
  - 128B line, 4 32B sectors
- One sector fetched per cycle
  - Up to 8 instructions
- 32 instruction fetch buffer
  - 8 instructions in
  - 5 instructions out
- 128 instruction prefetch buffer

| | latency |
|---|---|
| L1 I hit | 0 |
| L1 I miss, prefetch hit | 3 |
| L1 I miss, L2 hit | 12 |
| Branch taken | 2 |



# Branch Processing

- Up to 2 branches/cycle predicted
- Branch direction predicted by two-level (3 array) BHT
- Target address predicted by link stack (bclr) and count cache (bcctr)
- Mispredicted branch delays instruction issue by 12 cycles
- Extension to the branch instruction supports static branch prediction

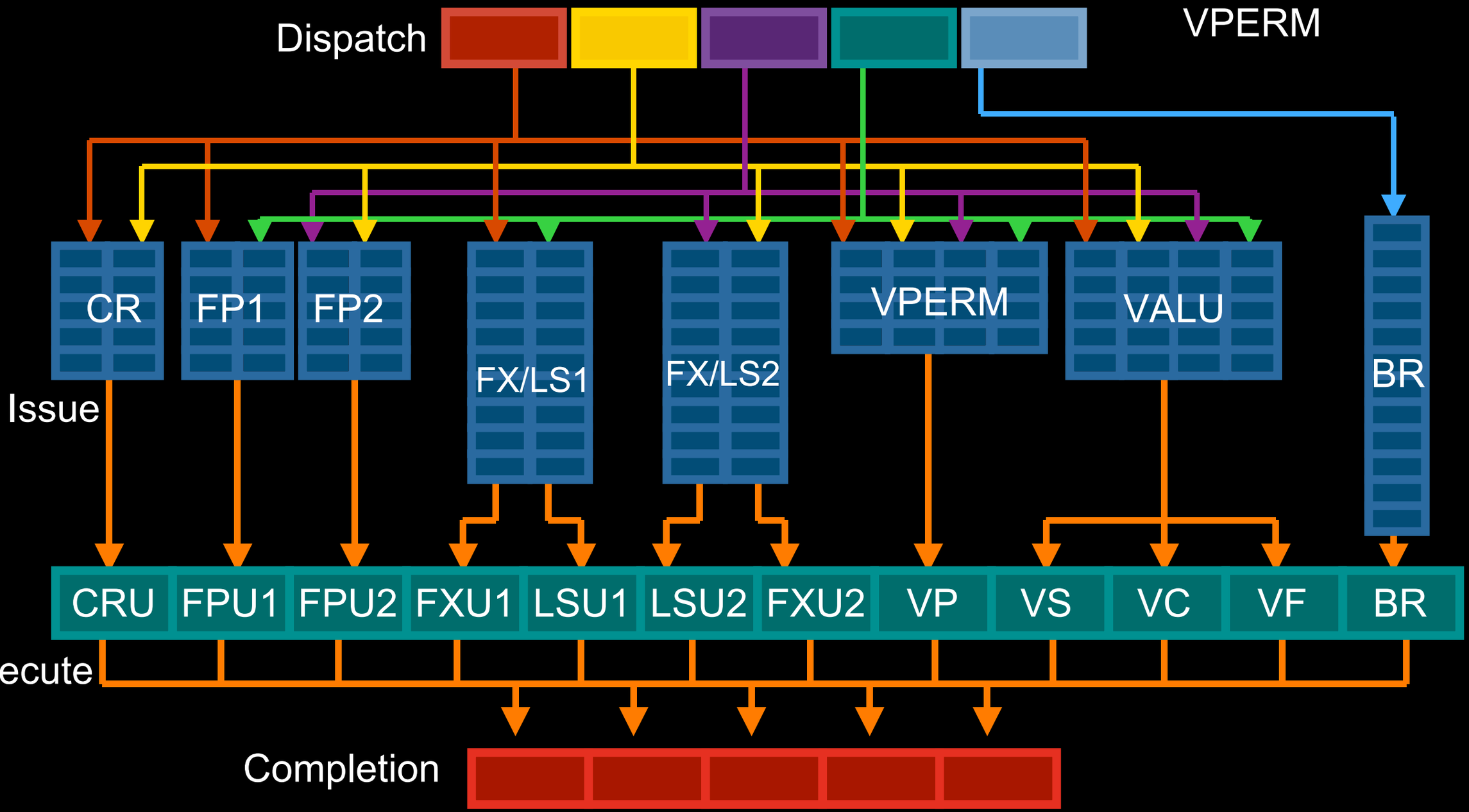


# Instruction Decode

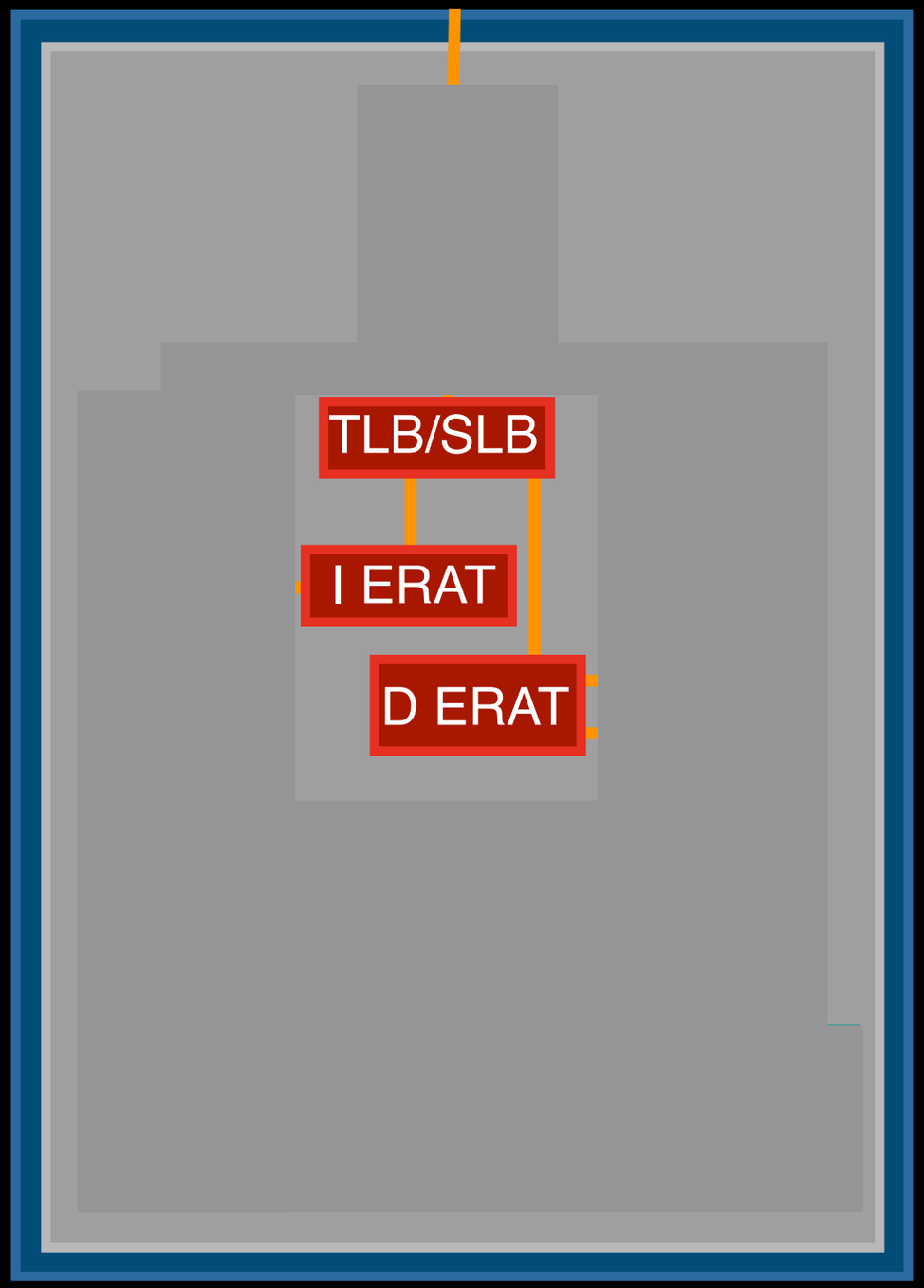
## Three types of instruction

- **Simple:** expressed as a single internal op
  - addi, lwz, vaddfp
- **Cracked:** composed of two iops
  - ldu, srw.
- **Microcoded:** composed of more than 2 iops
  - lhau, addc.,lmw, misaligned loads and stores

# Instruction Issue Queues

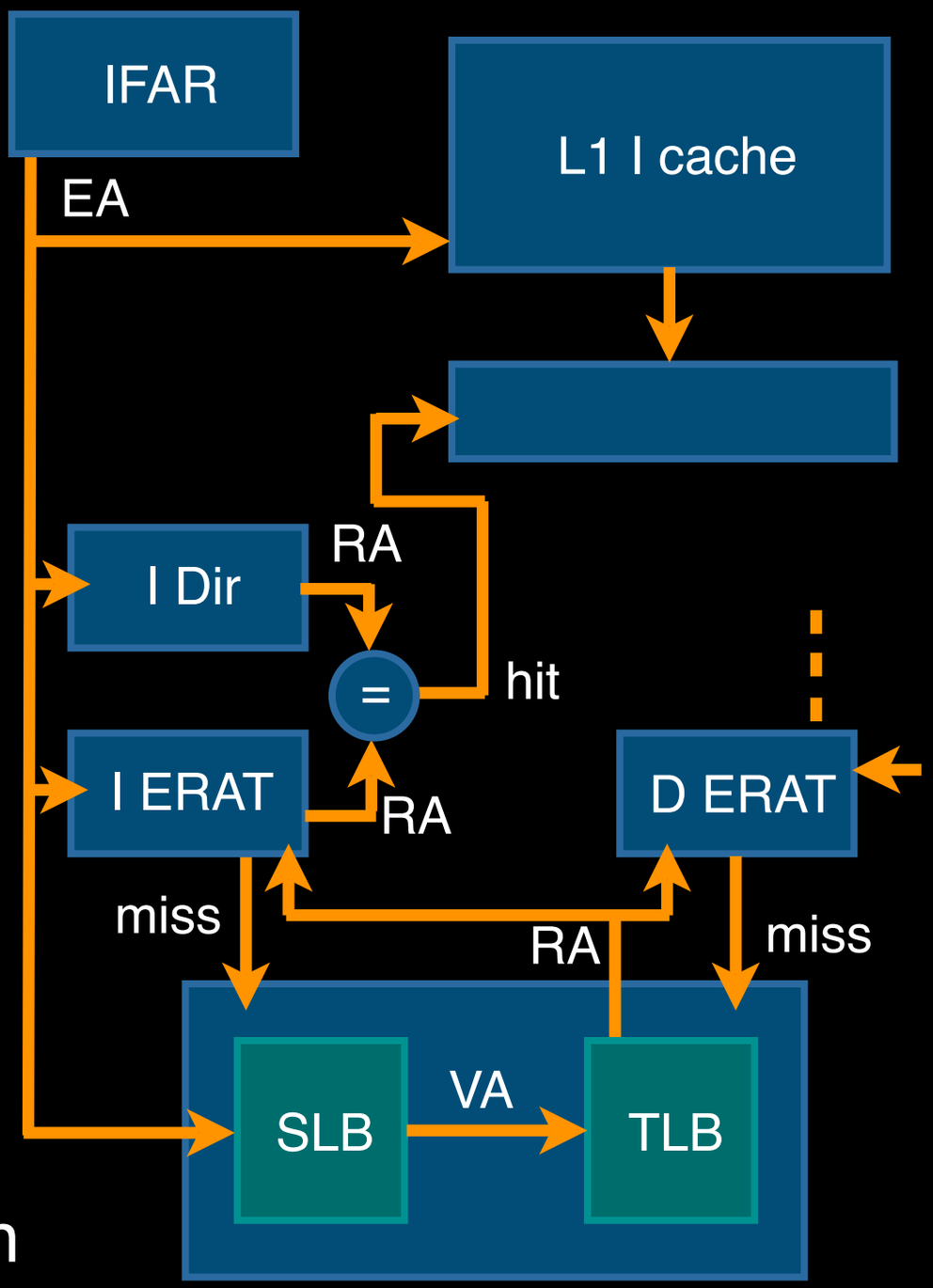


# Address Translation (MMU)

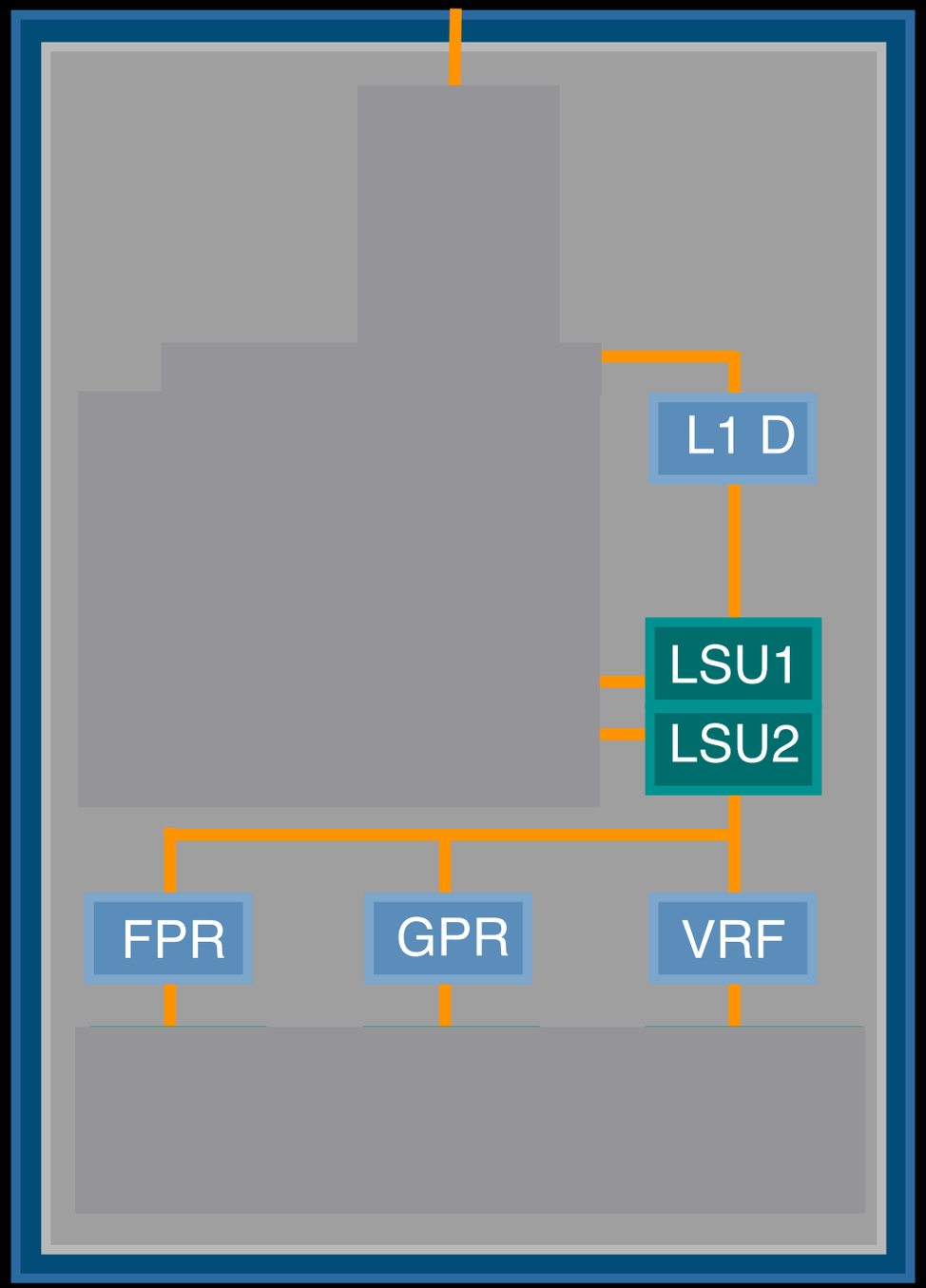


# Memory Management

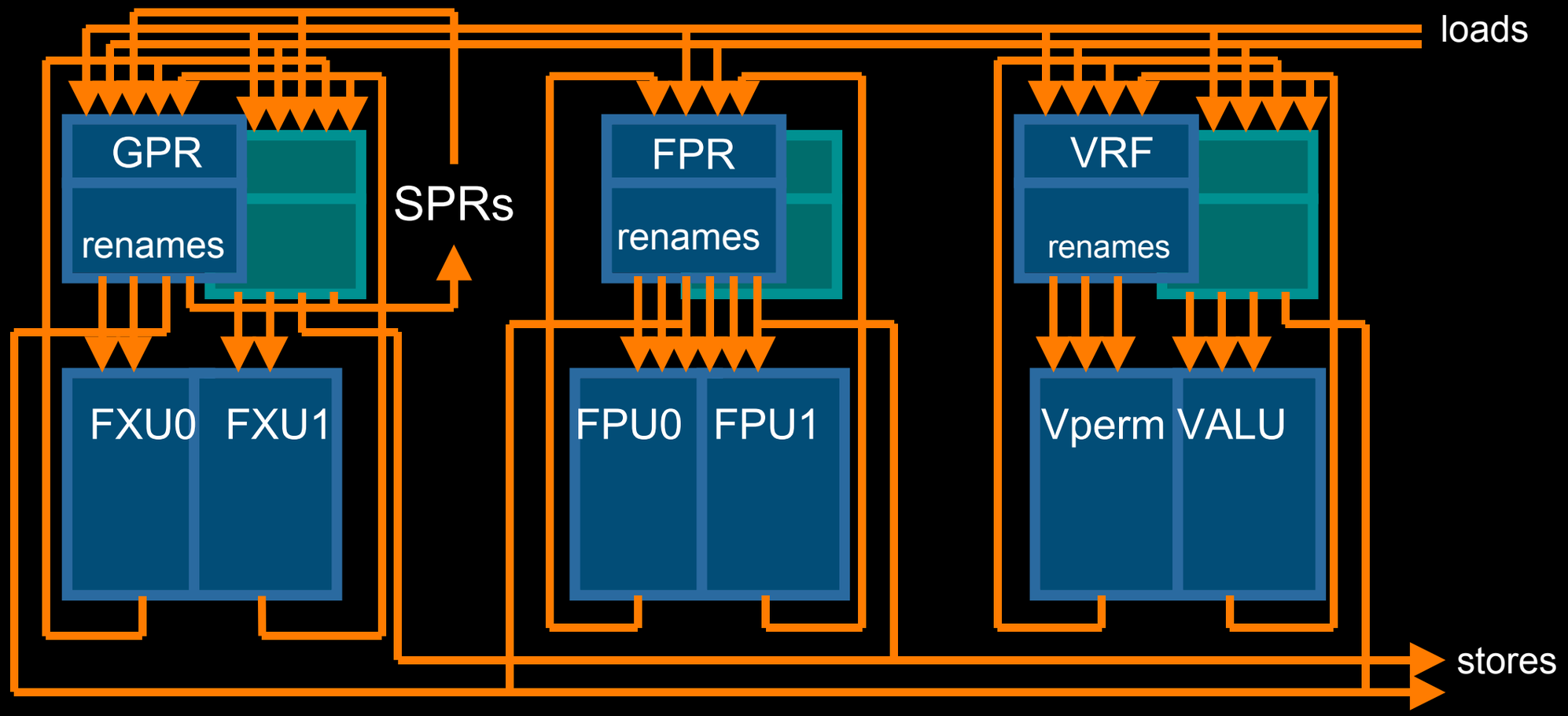
- Segmented, paged virtual memory
  - Segment table maps EA to VA
  - Page table maps VA to RA
  - ERAT caches EA to RA mappings
  -
- Arrays (MMU caches)
  - Segment Lookaside Buffer
    - 64 entry, translates 16GB
  - Table lookaside buffer
    - 4 x 256 entry, translates 16 GB
  - Effective to Real Address Translation
    - 2 x 64 entry, translates 512 KB



# Data Processing



# Load-store, Registers

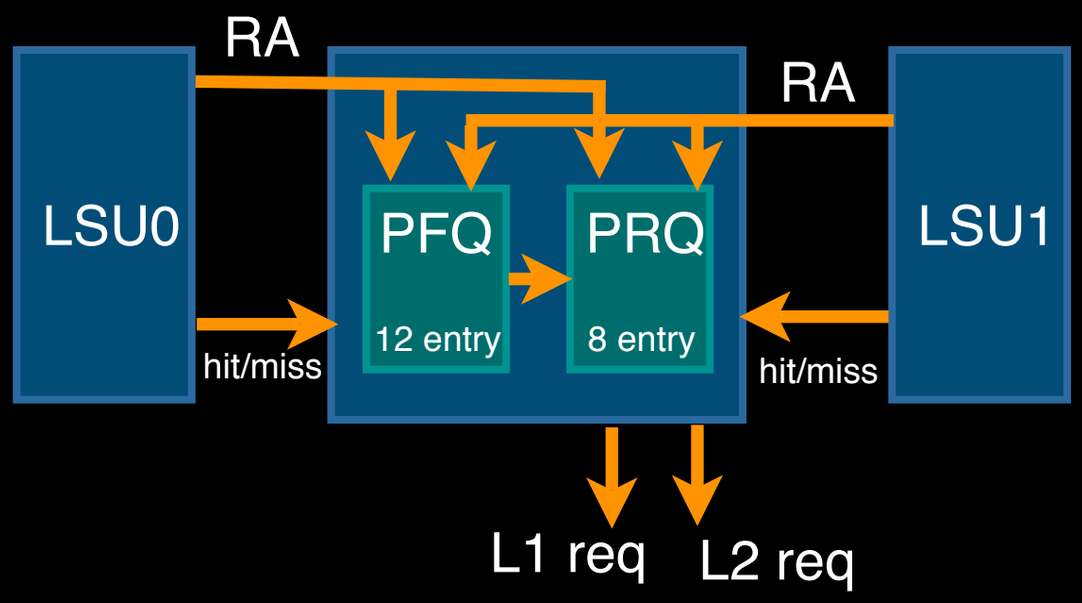



## Issue to issue latencies

| From | Load | FXU | FPU | VALU | VPERM |
|---|---|---|---|---|---|
| Load | 3 | 3 | 5 | 5 | 4 |
| FXU | | 2 | | | |
| FPU | | | 7 | | |
| Vsimple | | | | 2 | 3 |
| Vcomplex | | | | 5 | 6 |
| Vfloat | | | | 8 | 9 |
| Vperm | | | | 3 | 2 |

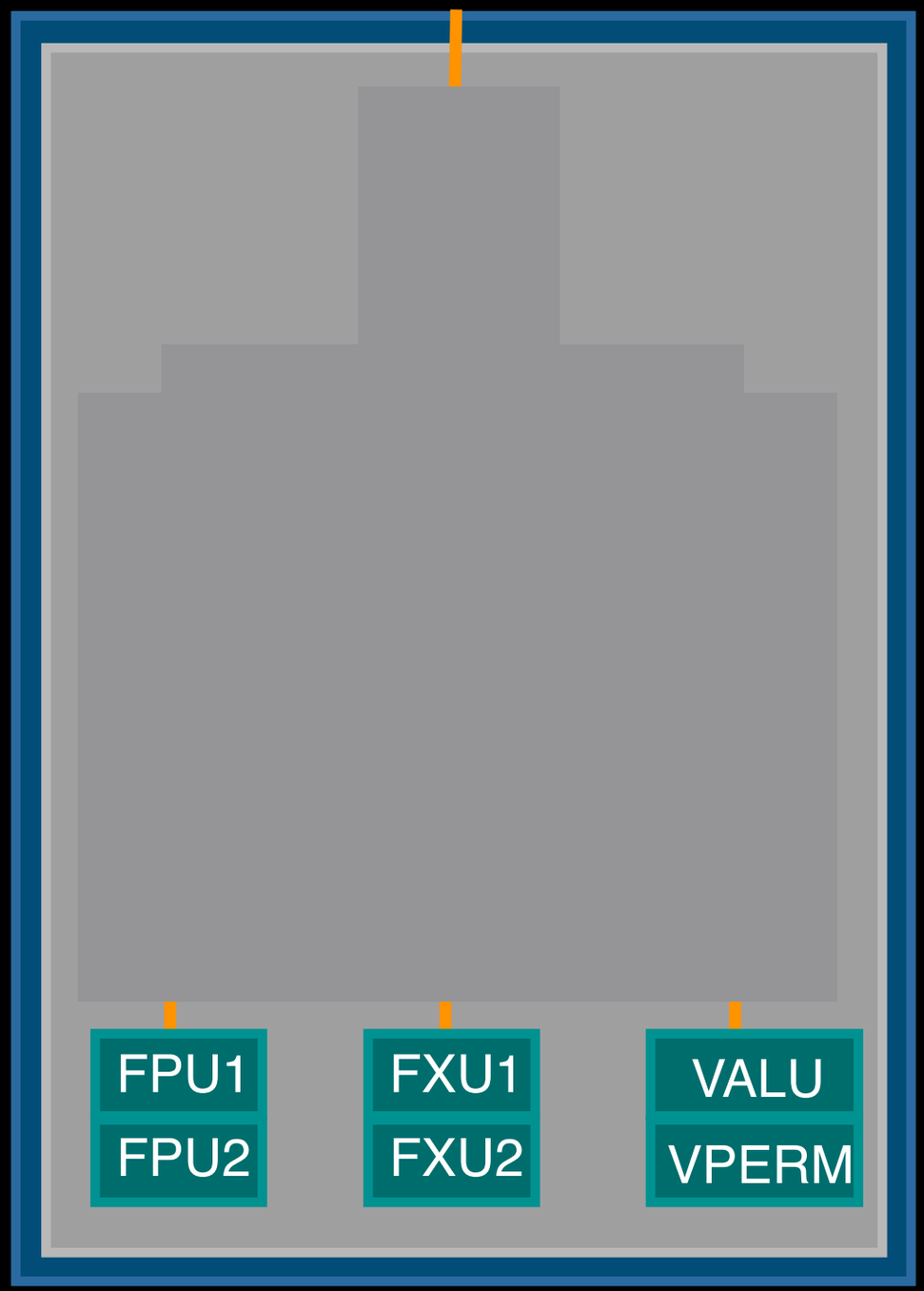
# Data Prefetch

- Three prefetch mechanisms all share common hardware
- Eight active data streams
  - 4 for dst, 4 for HW or all 8 for HW
- Stream initiation
  - Pattern of L1 D cache Load misses
  - Instruction–dcbt, dst
- Steady state
  - L1 prefetches one line ahead
  - L2 prefetches four lines ahead




| Instruction | Initiation | Pace | Terminate |
|---|---|---|---|
| - | HW | Demand | Page, LRU |
| dcbt | SW | Demand | Page, LRU |
| dst | SW | Async | Page, SW |

# Computation



# Integer, Float and Vector Units

FXU1
- Arithmetic
- Logical
- Shift/rotate
- Multiply
- mtspr/mfspr

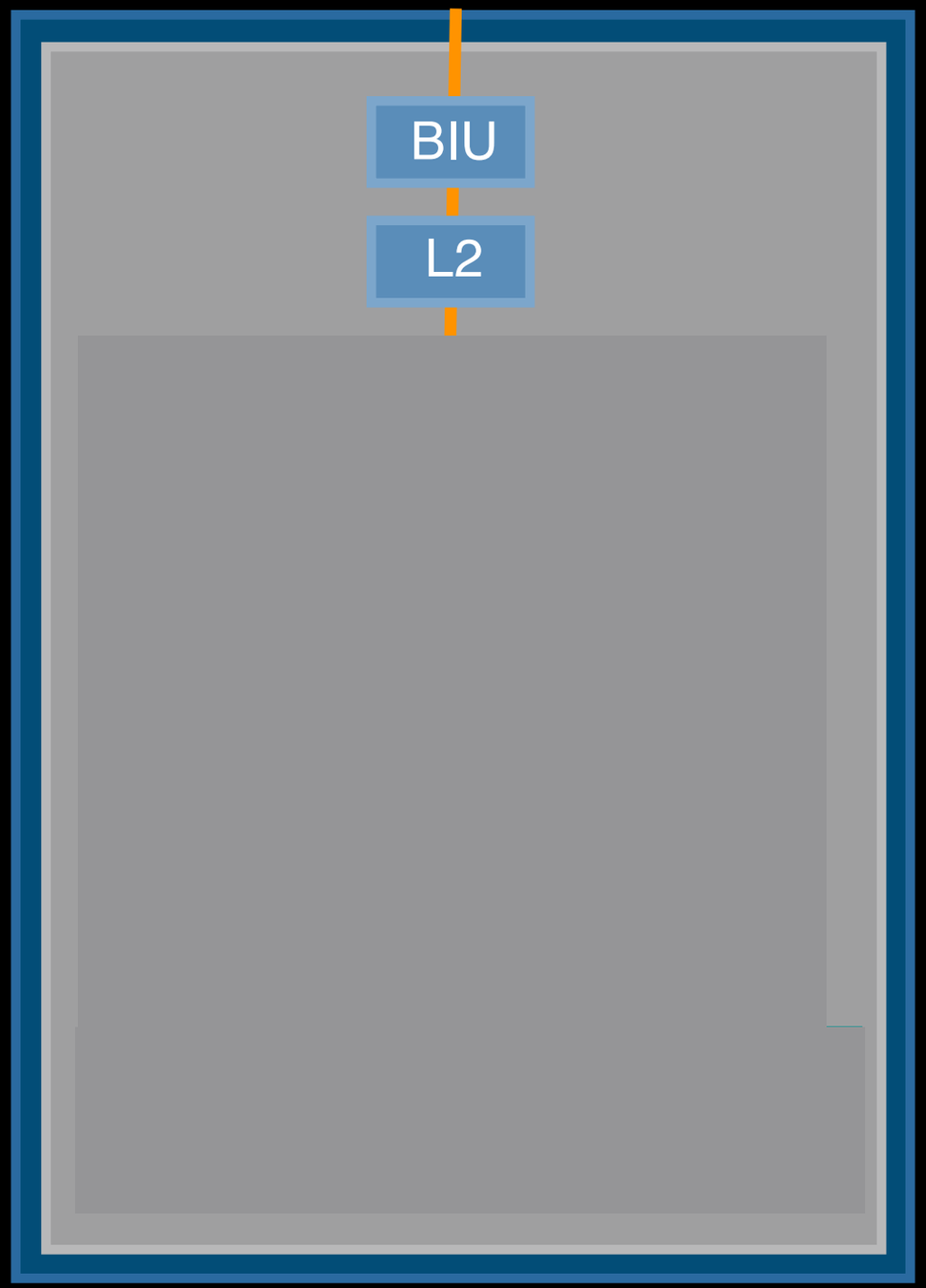
FXU2
- Arithmetic
- Logical
- Shift/rotate
- Multiply
- div

FPU1/FPU2
- Single-precision
- Double-precision
- Denorms
- NaNs
- Exceptions
- fsqrt,fsqrts,fsel
- fres,frsqrte
- No non-IEEE mode

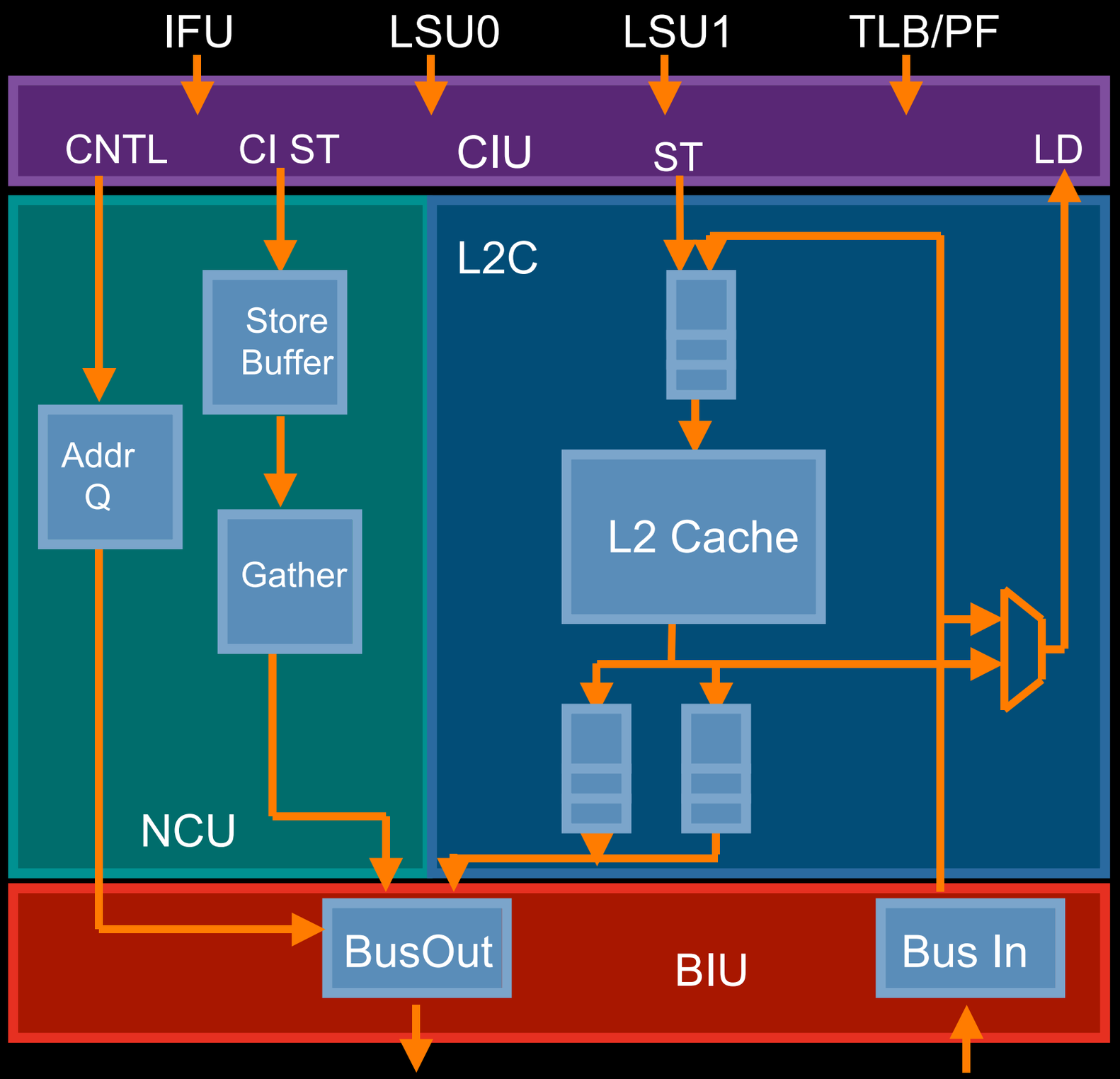
VPERM
- Permute
- Merge
- Splat
- Pack

VALU
- Simple
- Complex
  -Multiply
  -Sum across
- Float

# L2 and Bus Interface

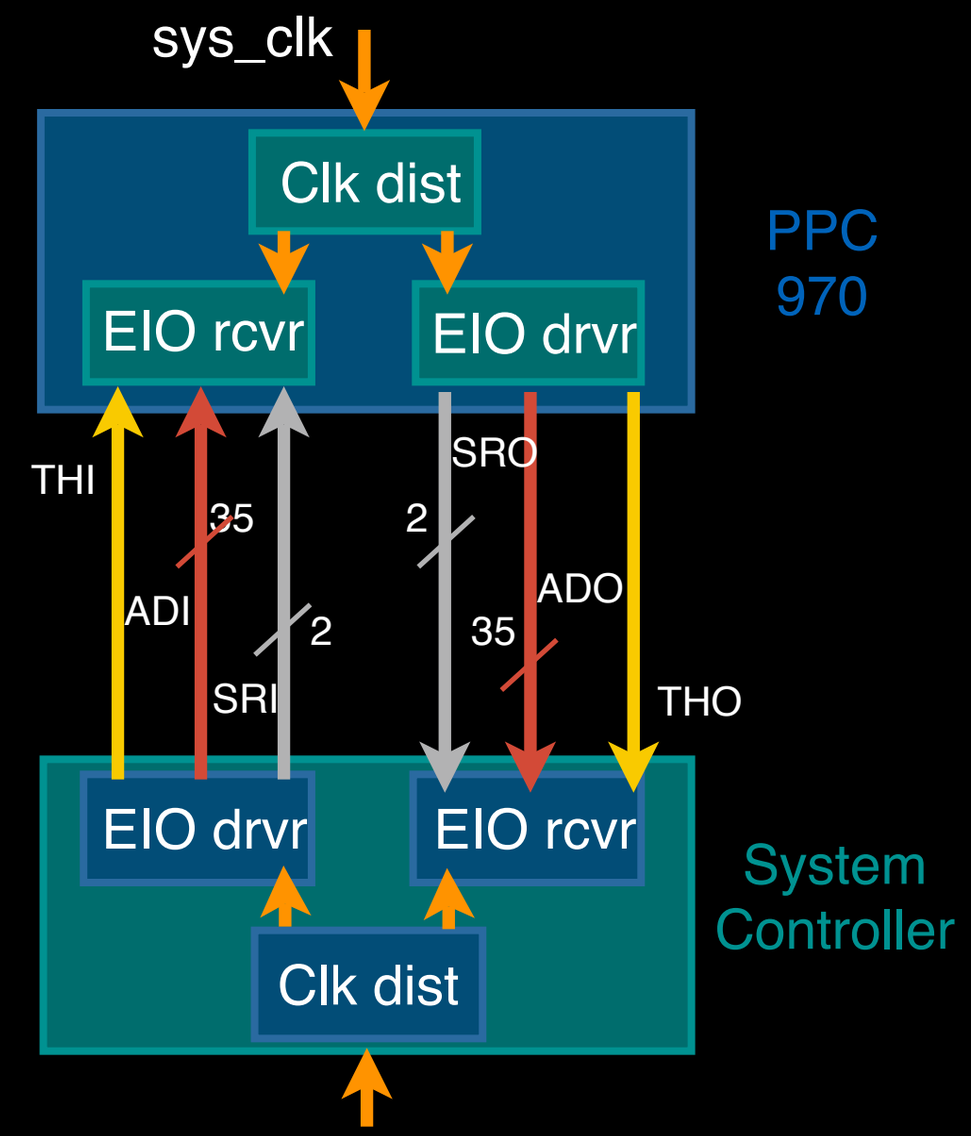


# Memory Subsystem

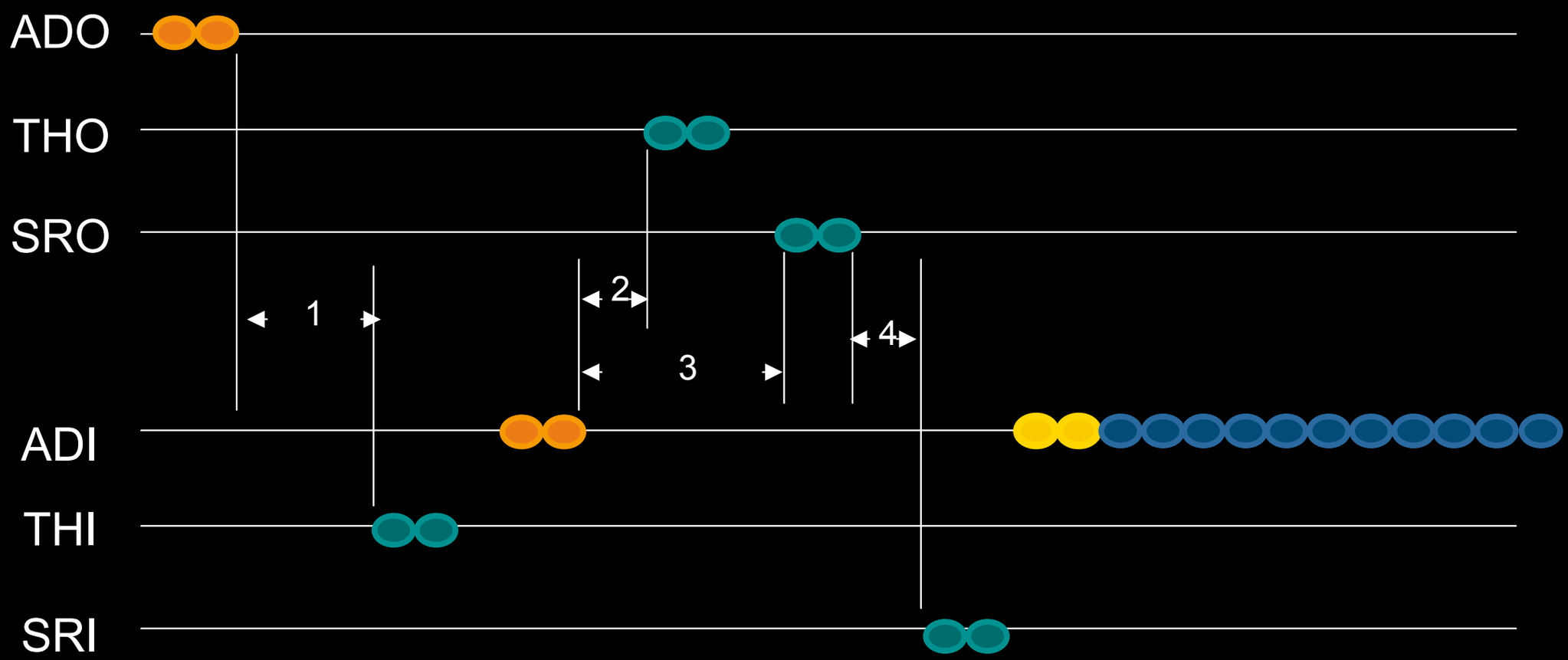


# High-Bandwidth Processor Bus

- Electrical Interface
  - Two 4B, pt-pt, src sync busses
  - Initialization alignment deskews bits
- Logical interface
  - Pipelined, out-of-order transactions
  - Address/command packets
    - Three types—Read, Write, Control
    - 42 bit addr, TType, TSIZ, WIMG, tag
  - Data packets are
    - 4B x 2,4,8,16,32 beats



# Bus Example—Read Transaction

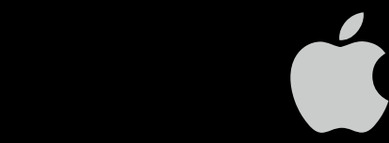



1 – STATLAT(P) cycles
2 – Fixed by STATLAT(SC) cycles
3 – SNOOPLAT cycles
4 – SNOOPACC cycles

Read command packet
Read-data packet header
Read data beat
Handshake or snoop response

# PowerPC 970 Feature Summary

- High-performance, superscalar, out-of-order, 64-bit design
  - 2 GHz processor, 5 completions/cycle
  - 100 instructions in execution, >200 in flight
  - Full 64-bit implementation, native support for 32-bits
- Instruction fetch, decode, dispatch, issue
  - 8 fetch, 5 dispatch, 10 issue, highly accurate branch prediction
- High computational throughput
  - Dual fixed point, dual floating point, dual vector units
  - Dual load-store, data prefetch
- High-speed bus to memory and I/O
  - Pipelined, out-of-order transactions
  - 1 GHz data rate, 8 GB/s memory and I/O bus



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